Proposition de sujet de thèse – 2019 / 2020
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Référence : STH-2019-06

Équipe de recherche de la fédération 1 (porteuse du sujet) 3 -- SCALP

Équipe de recherche de la fédération 2 (le cas échéant)

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HDR X Oui, délivrée le 20 Mai 2019 par l'INP Toulouse
☐ Non

Ecole doctorale de rattachement EDMITT

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HDR ☐ Oui, délivrée le..... par.....
x Non

Ecole doctorale de rattachement EDMITT

Compléter le dossier en suivant la trame ci-dessous

1. Sujet de thèse (1 à 2 pages)

- Titre

Predictable real-time systems with multi-core implementations

- Description

This PhD thesis proposal is about the configuration and the study of multi-core, many-core, and GPU systems, and make predictability out of such platform for safety-critical real-time applications.

Predictable task execution relates to the identification and the guarantees of reproducible execution conditions. The PhD candidate will have to investigate the interactions among tasks and system elements, the dependencies that exist within multiple core systems (multi-core, many-core, and GPUs) due to parallel executions and shared resources, and the interference that shared resources create on tasks executions. In fewer words, the student will characterize and control the impact of real-time operating systems and HW parameters on the task execution behavior.

The models of system resources and the underlying hardware will be exploited in terms of effects on task executions under different execution conditions, worst-case included. There will be applied already existing

metrics and developed new one to evaluate system predictability. Among them, task execution time (average behavior) and task worst-case execution time (worst-case behavior) will be considered, [1]. Other system parameters that relates to resource usage (bus and memory) will be considered to define contention effects on tasks and system predictability. The interference received from concurrent tasks and system components will be characterized and guaranteed (certified).

The student will apply both statistical and deterministic approaches to predictability [2,3,4a]. He or she will develop analytic and statistical analysis tools to be used in the predictability evaluation.

The PhD thesis will also consider placement and schedulability techniques to avoid or reduce interference among the different system components. The timing analysis formerly outlined will be used for evaluating such techniques, as well as for evaluating partitioning capabilities from operating systems and hypervisors.

Within the thesis, an iterative approach to interference and predictability analysis is developed: at first there is the interference identification, then the design of benchmarks able to exercised/stress the interferences [10], and the analysis to validate that. Finally, system design mechanisms are developed to avoid or reduce interference effects.

With this thesis, the focus is on multi-core processors like [5a], many-core processors like [6,7], and GPUs like [11]. The software development instead is done in the context of the existing SchedMCore framework [8], Kalray frameworks [7] and PikeOS [9].

The candidate will face the configuration parameters and the underlying execution system to identify interferences to task executions. He/she will also document and automatize the procedure to execute tasks implemented as C functions, for realistic system implementations as well as realistic system interferences. The thesis will focus on safety-critical embedded system with many-cores applied in avionic (safety-critical systems) or non-critical applications (image processing, video, robotic, etc.), where to develop the models and the analyses. Mixed-critical applications, dependence and concurrent execution effects will be investigated.

[1] *Learning from Probabilities: Dependences within Real-Time Systems*
Alessandra Melani, Eric Noulard and Luca Santinelli; ONERA Toulouse
18th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2013).

[2] *The Worst-Case Execution-Time Problem—Overview of Methods and Survey of Tools*,
Reinhard Wilhelm et al., ACM Trans. Embed. Comput. Syst., Vol. 7, Issue 8, May, 2008.

[3] Revising Measurement-Based Probabilistic Timing Analysis
Luca Santinelli, Fabrice Guet, Jérôme Morio, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2017)

[4] *Tilera processor family* : "http://www.tilera.com/"http://www.tilera.com

[4a] RAPITA systems "https://www.rapitasystems.com/products/rapitime"https://www.rapitasystems.com/products/rapitime

[5a] NXP T4240 ,"https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/qoriq-platforms/t-series/qoriq-t4240-t4160-t4080-multicore-communications-processors:T4240"https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/qoriq-platforms/t-series/qoriq-t4240-t4160-t4080-multicore-communications-processors:T4240

[5a] Keystone II, http://www.ti.com/product/AM5K2E02

[6] *Tilera processor family* : "http://www.tilera.com/"http://www.tilera.com/

[7] *Kalray MPPA processor* : "http://www.kalray.eu/en/products/mppa.html"http://www.kalray.eu/en/products/mppa.html

[8] *SchedMCore* : "http://sites.onera.fr/schedmcore"http://sites.onera.fr/schedmcore

[9] *PikeOS* : "https://www.sysgo.com/products/pikeos-hypervisor/"https://www.sysgo.com/products/pikeos-hypervisor/

[10] Multi-core microbench technology, "https://www.bsc.es/research-and-development/software-and-apps/software-list/multi-core-microbenchmark-technology-mµbt"https://www.bsc.es/research-and-development/software-and-apps/software-list/multi-core-microbenchmark-technology-m%CE%Bcbt, Barcelona Supercomputing Center

[11] JETSON NVIDIA GPU, "https://www.nvidia.com/object/jetson-tk1-embedded-dev-kit.html"

- Contexte scientifique, situation par rapport à l'état de l'art

Interference analysis and more in general the study of the predictability for multi-core platforms, represent the trend for todays and future real-time systems. The statistical approach from measurements to build average and worst-case models is the only possibility seen the complexity of todays real-time systems implemented with multi-core and the impossibility of applying the more classical static timing analysis. On-going collaborations on the subject are with CISTER Porto, BSC Barcelone, Cobham Gaisler, RAPITA, etc. Are producing ANR project proposals (2019), ESA project proposal (2019), and H2020 project proposal (2019).

- Mise en évidence de l'aspect novateur, prospectif, de l'apport, de l'originalité

The innovation consist of developing statistical approaches to measurements of different parameters in order toderive average and worst-case models. This is a work already started at the ONERA DTIS/SEAS team with PR projects and ANR project like CAPHCA.
This work has started with a Master stage and initial results will be published on rank A conferences and technical reports.
The ISAE is contributing with implementation aspects, the knowledge of interference with communication bus, and scheduling/placement aspects.
The originality consists on 1) identification of interference (from the Phylog ONERA project applied to specific multi-core processors), 2) the imodels to be developed with quantification and qualification of interference, 3) correlation and parametric analysis between different parameters. Also, important contribution and originality is from the development of ad-hoc benchmarks to make parametric interference for specific multi-core platforms. Finally, with those statistical approaches, we can qualify hypervisors and partitioning qualities, which is an absolute original contribution

2. Profil du Candidat

- Formation et spécificités souhaitées –

- Laboratoire(s) d'accueil envisagé(s)

  Federation ISAE-ONERA, Thematique 3 - Systèmes critiques à logiciel prépondérant (ingénierie systèmes embarqués)

- Ecole doctorale de rattachement envisagée

  EDMITT – Université Paul Sabatier

3. Partenariats et financement

- Partenariat industriel ou académique envisagé

RAPITA York, CISTER/ISEP Portugal, Barcelona Supercomputing Center

- Types de financement demandés ou visés : fédération, EUR TSAE, DGAC, DGA, région, CNES, MESR, Ecole doctorale, CIFRE, Projet Européen….

Federation, DGA (PEA DRONE)

4. Thèses en cours d'encadrement par le ou les directeur(s) de thèse
(préciser pour chaque encadrement : le nom du doctorant, l'année de thèse, le sujet, le financement et l'école doctorale)

Jasdeep Singh, ONERA thèse. En 2019 au troisième année.

5. Commentaire, avis motivé des représentants des équipes de la fédération porteuses du sujet
(justifier le choix du sujet et son positionnement au sein de l'équipe)

6. Pièces jointes éventuelles
(par exemple CV de candidats pressentis, sujet tel que déposé dans un établissement, ...)