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THE FRENCH AEROSPACE LAB

## PROPOSITION DE POST-DOCTORAT

**Intitulé : Interference analysis for hybrid architectures**

Référence : **PDOC-DTIS-2023-05**
*(à rappeler dans toute correspondance)*

| **Début du contrat :** 2023 | **Date limite de candidature :** |
|---|---|

**Durée : 12 mois, éventuellement renouvelable une fois - Salaire net : environ 25 k€ annuel**

**Mots clés**

Certification of multi-core platforms, real-time systems, formal modelling and analysis

**Profil et compétences recherchées**

Low level programming in multi-core COTS (C and assembly). OpenCL will be a plus.

Real-time systems programming

Some knowledge on formal methods is welcome

**Présentation du projet post-doctoral, contexte et objectif**

The post doc position will be part of an ANR-DFG project named InterMCore (2023-2026) with 3 partners (CEA List, TU Dresden, TU Dortmund).

**Context** Safety-critical systems must be carefully developed by assessing the safety and even in some domains to comply with some standards. The project targets both the automotive and the aeronautics domains. As a consequence, the applicable standards are:

- ISO2626.2 [1] that provides guidance to ensure that hardware and software components are developed with an appropriate level of rigorous design,
- AMC 20.193/CAST-32A [2] (formerly CAST-32A) which provides guidance for embedding multi-core COTS in avionic platforms.

In the project, we focus on the *embeddability* of *high-performance hybrid COTS platforms* when targeting next generation applications, mixing different criticality requirements, or different programming paradigms (e.g., control/command applications with ML-based applications). *Hybrid architectures / platforms* refer to chips integrating several (possibly heterogeneous) cores interconnected by a communication medium (such as a shared bus or a hierarchy of shared buses or a network on chip or a combination of them) and a set of dedicated accelerators (e.g. GPU or ASIC). The term *embeddability* must be understood here in the sense of applicability of standards.

**Project objective** While existing works often focus on one aspect when dealing with interference like identifying structural hardware interferences or timing anomalies during the WCET timing analysis, there is a clear lack of a combined (software and hardware) methodology-aware development for the analysis and mitigation of interference for complex COTS multi-core hybrid architectures. We thus aim at building such a global software/hardware interference-centric methodology to support the design of next generation of automated driving and avionics systems by:

1. applying both formal methods and benchmarking to model and assess the timing behavior and predictability of these applications over MPSoCs;
2. defining appropriate rules and transformations to guide the application software synthesis for an enhanced timing behavior, i.e. with reduced interferences.

The proposed approach is illustrated in Figure 1.

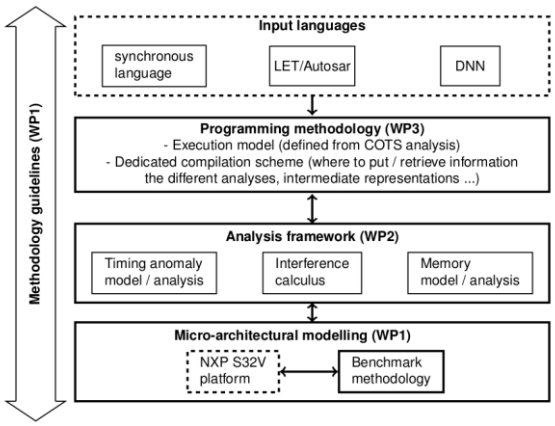


*Figure 1: overview of InterMcore approach*

**Post doc objective** Within InterMCore, ONERA will be in charge of developing the benchmark methodology based on previous works done in PHYLOG [3] and many other projects e.g. [4,5]. The purpose will be to adapt existing micro-benchmarks to estimate the cost of interferences on the platform, exercising the various interference channels, and in particular to consider and compare *accelerators* such as GPU [6,7,8] or SIMD CPU extensions [10, 11]. The work will also have to consider the input languages and execution frameworks in order to identify application profiles. The work of [9] provides an example of an approach to characterize a platform considering the applications.

The output of defining and applying the benchmark methodology will be a clear characterization of the target NXP S32V234 platform [12], and the capacity to derive a valid, tight model of the platform that will allow formal analysis [13, 16]. A second contribution of the post doc will concern the modelling and interaction with the (partners) analysis methodology. The work will iterate over the model and the benchmarks in order to provide accurate information to the analyses, and assess the impact of proposed methods to mitigate interferences [14, 15] and cope with timing anomalies [17,18].

In addition, the post doc fellow will have to:

- Participate to the project meetings
- Collaborate with the partners on the modelling of the platform
- Help develop the InterMCore methodology

**References**

[1] Road vehicles - Functional safety, ISO 26262:2018: ISO, Geneva, Switzerland.

[2] Certification Authorities Software Team, Multi-core Processors - Position Paper.

[3] Frédéric Boniol et al., “PHYLOG certification methodology: a sane way to embed multi-core processors,” in 10th European Congress on Embedded Real Time Software and Systems (ERTS 2020), 2020. https://w3.onera.fr/phylog/

[4] Jeremy Giesen et al. “PRL: Standardizing Performance Monitoring Library for High-Integrity Real-Time Systems” IEEE 39th International Conference on Computer Design (ICCD) 2021

[5] Roger Pujol et al. « Empirical Evidence for MPSoCs in Critical Systems: The Case of NXP's T2080 Cache Coherence ». Design, Automation & Test in Europe Conference & Exhibition (DATE). 2021

[6] Jon Perez-Cerrolaza et al. « GPU Devices for Safety-Critical Systems: A Survey ». ACM Computing Surveys (CSUR) 2022.

[7] Tanya Amert et al. TimeWall: Enabling Time Partitioning for Real-Time Multicore+Accelerator Platforms. RTSS 2021

[8] Tanya Amert et al. CUPiDRT: Detecting Improper GPU Usage in Real-Time Applications. ISORC 2021: 86-95

[9] Antonio Paolillo et al. “Porting a safety-critical industrial application on a mixed-criticality enabled real-time operating system” in 9th European Congress on Embedded Real Time Software and Systems (ERTS 2020), 2018.

[10] https://www.arm.com/technologies/neon

[11] Roger Pujol et al. Vector Extensions in COTS Processors to Increase Guaranteed Performance in Real-Time Systems. ACM Trans. Embed. Comput. Syst. 2022.

[12] https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/s32-automotive-processors/s32v2-processors-for-vision-machine-learning-and-sensor-fusion:S32V234

[13] F. Boniol et al. Deterministic execution model on COTS hardware. In 25th International Conference Architecture of Computing Systems (ARCS'12)

[14] Q. Perret. Predictable execution on many-core processors. Thèses, INSTITUT SUPERIEUR DE L'AERONAUTIQUE ET DE L'ESPACE (ISAE) ; UNIVERSITE DE TOULOUSE, Apr. 2017.

[15] S. Saidi et al. "The shift to multicores in real-time and safety-critical systems," 2015 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2015

[16] S. Saidi and A. Syring. Exploiting locality for the performance analysis of shared memory systems in mpsocs. In 2018 IEEE Real-Time Systems Symposium, RTSS 2018.

[17] Benjamin Binder, Mihail Asavoae, Florian Brandner, Belgacem Ben Hedia, Mathieu Jan. Formal modeling and verification for amplification timing anomalies in the superscalar TriCore architecture. Int. J. Softw. Tools Technol. Transf. 24(3): 415-440 (2022)

[18] Benjamin Binder, Mihail Asavoae, Belgacem Ben Hedia, Florian Brandner, Mathieu Jan: Is This Still Normal? Putting Definitions of Timing Anomalies to the Test. RTCSA 2021: 139-148

**Collaborations extérieures**

Partners of InterMCore : CEA List, TU Dresden, TU Dortmund

**Laboratoire d'accueil à l'ONERA**

Département : Traitement de l'Information et Systèmes

Lieu (centre ONERA) : Toulouse

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